

What is Claimed is:

1. A semiconductor device comprising an n-channel field effect transistor and a p-channel field effect transistor, said both transistors being provided on a common base-substrate, wherein

add #17
00802T-120800
a surface region, in which said n-channel field effect transistor is provided, of said base-substrate comprises: a silicon substrate; a buffer layer formed on said silicon substrate, said buffer layer being made from a silicon-germanium compound having a germanium concentration gradually increased toward an upper surface of said buffer layer; a relax layer formed on said buffer layer, said relax layer being made from a silicon-germanium compound having a germanium concentration nearly equal to that of a surface portion of said buffer layer; and a silicon layer formed on said relax layer, and wherein

a surface region, on which said p-channel field effect transistor is provided, of said base-substrate, comprises: said silicon substrate; a silicon-germanium compound layer formed on said silicon substrate; and a cap layer formed on said silicon-germanium compound layer, said cap layer being made from silicon.

2. A semiconductor device according to claim 1,

wherein source/drain regions of said n-channel field effect transistor are formed in said silicon layer, and source/drain regions of said p-channel field effect transistor are formed in said silicon-germanium compound layer.

3. A method of fabricating a semiconductor device in which an n-channel field effect transistor and a p-channel field effect transistor are provided on a common base-substrate, said method comprising the steps of:

etching a surface layer of an n-channel region, in which said n-channel field effect transistor is to be formed, of a silicon substrate, to form a stepped recess at said n-type region;

forming a buffer layer made from a silicon-germanium compound having a germanium concentration gradually increased toward an upper surface of said buffer layer on said silicon substrate;

forming a relax layer made from a silicon-germanium compound having a germanium concentration nearly equal to that of a surface portion of said buffer layer on said buffer layer;

forming a silicon layer on said relax layer;

removing said silicon layer, said relax layer, and said buffer layer in a p-type region, on which a p-

09733474-120800
Cul B3

channel field effect transistor is to be formed, of said silicon substrate, by etching using a resist pattern as a mask;

forming a silicon-germanium compound layer on both said silicon substrate and said silicon layer;

planarizing the surface of said silicon-germanium compound layer in a state that said silicon layer is exposed in said n-type region and said silicon-germanium compound layer is left in said p-type region;

forming a silicon epitaxial layer on both said silicon layer and said silicon-germanium compound layer, to form a silicon layer composed of said silicon layer and said silicon epitaxial layer in said n-type region, and to form a cap layer composed of said silicon epitaxial layer in said p-type region; and

forming gate electrodes on said silicon layer in said n-type region and on said cap layer in said p-type region via a gate insulating film, and forming n-type source/drain regions in said silicon layer and p-type source/drain regions in said silicon-germanium compound layer.